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Document Number 72

Entry 72 of 191 File: DWPI Sep 22, 1998

DERWENT-ACC-NO: 1998-531247
DERWENT-WEEK: 199845

TITLE: Computer based gate level specification generation method for design, verification and implementation of ASCI - involves generating synthesis script that specifies characterizing of synthesised lower level module according to user specified constraints

INVENTOR: ADKAR, S; GUPTE, V V

PATENT-ASSIGNEE: ; LSI LOGIC CORP[; LSILN]

PRIORITY-DATA:
1996US-0683287 July 18, 1996

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5812416 A	September 22, 1998	N/A	031	G06F017/50

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-NO
US 5812416A	July 18, 1996	1996US-0683287	N/A

INT-CL (IPC): G06F 17/50

ABSTRACTED-PUB-NO: US 5812416A
BASIC-ABSTRACT:

The method involves receiving the user-specified constraints and a programming language description of the IC. At least one synthesis script for the IC is generated.

The synthesis script specifies synthesizing of lower level modules and top level modules according to default constraints and user specified constraints, respectively. Further the synthesis script specifies characterizing of the synthesised lower level module according to user specified constraints.

ADVANTAGE - Enables to store design information for utilization by design applications. Uses authorization file for restricting modification of design information without necessary security access.

CHOSEN-DRAWING: Dwg.14/19

TITL E-TERMS: COMPUTER BASED GATE LEVEL SPECIFICATION GENERATE METHOD DESIGN VERIFICATIO N IMPLEMENT GENERATE SYNTHESIS SCRIPT SPECIFIED SYNTHESIS LOWER LEVEL MODULE ACCORD USER SPECIFIED CONSTRAIN

DERWENT-CLASS: T01

EPI-CODES: T01-J15A1; T01-J15A2; T01-J15B;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1998-414526

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